



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. .... 09/885,393  
Confirmation No. .... 4911  
Filing Date .... June 19, 2001  
Inventor .... Richard Holscher et al.  
Assignee .... Micron Technology, Inc.  
Group Art Unit .... 1756  
Examiner .... Unknown  
Attorney's Docket No. .... MI22-1694  
Customer No. .... 21567  
Title: Semiconductor Processing Methods

**INFORMATION DISCLOSURE STATEMENT**

References -- See Attached Form PTO-1449

The attached Form PTO-1449 is submitted in compliance with 37 CFR §1.56. No admission is made regarding whether the submitted references are prior art.

This Information Disclosure Statement is being filed within three months of the filing of the application or before the mailing of a first Office Action on the merits, whichever occurs last. Therefore, no fee is believed to be required. However, in the event that a fee is required for filing this Information Disclosure Statement, please charge the fee specified under 37 C.F.R. Section 1.17(p) to Deposit Account No. 23-0925. Please credit Deposit Account No. 23-0925 with any overpayment of the above fee.

Respectfully submitted,

Dated: 1/13/04

Attorney: 

Robert C. Hyta  
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**EL979978767**

Form PTO-1449		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. M122-1694		SERIAL NO. 09/885,393	
LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)				APPLICANT Richard Holscher et al.			
				FILING DATE June 19, 2001		GROUP 1756	
U.S. PATENT DOCUMENTS							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	6,518,122	02/03	Chan, et al.			
	AB	6,492,688	12/02	Ilg (ILG)			
	AC	6,373,114	04/02	Jeng, et al.			
	AD	2001/0019868	09/01	Gonzalez, et al.			
	AE	6,503,818 B1	01/03	Jang			
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	AK	6,435,943 B1	08/02	Chang, et al.			
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	AM	6,284,677 B1	09/01	Hsiao, et al.			
	AN	6,030,901	02/00	Hopper, et al.			
FOREIGN PATENT DOCUMENTS							
		Document Number	Date	Country	Class	Subclass	Translation
							Yes No
	AM	8046186	02/96	JP			
	AN	8046188	02/96	JP			
	AO	7201716	08/95	JP			
	AP	6232113	08/94	JP			
OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)							
	AR		Wolf, S., "Silicon Processing for the VLSI Era." Vol. 1, pps. 407-413.				
	AS		Wolf, S., "Silicon Processing for the VLSI Era". Vol. 2, pgs. 48-49 and 435.				
EXAMINER				DATE CONSIDERED			
<p>*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.</p>							

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U.S. PATENT DOCUMENTS								
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
	AA	6,133,618	10/00	Steiner				
	AB	5,994,217	11/99	Ng				
	AC	5,985,519	11/99	Kakamu, et al.				
	AD	5,747,388	05/98	Kusters, et al.				
	AE	5,639,687	06/97	Roman, et al.				
	AF	5,498,555	03/96	Lin				
	AG	2001/0003064	06/01	Ohto				
	AH	2003/0013311	01/03	Chang, et al.				
	AI							
	AJ							
	AK							
	AL							
	AM							
	AN							
FOREIGN PATENT DOCUMENTS								
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							Yes	No
	AM							
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